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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/978,185	10/15/2001	Chih-Hao Chen-hao	CENiX.009	3921

7590 03/14/2005

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EXAMINER	
CURS, NATHAN M	

ART UNIT	PAPER NUMBER
2633	

DATE MAILED: 03/14/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/978,185	CHEN-HAO, CHIH-HAO	
	Examiner	Art Unit	
	Nathan Curs	2633	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on *15 October 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-27* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 January 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. Figure 1 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.121(d)) so as not to obstruct any portion of the drawing figures. If the examiner does not accept the changes, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 5-8, 13, 14, 21 and 23 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Regarding claims 5-7, Applicant claims that "said first bus is an address based shared bus interface". Claiming that a bus is a bus interface makes the claim ambiguous.

Regarding claim 8, Applicant claims that "said second bus is an internal shared bus interface". Claiming that a bus is a bus interface makes the claim ambiguous.

Regarding claims 13 and 14, Applicant claims that "said at least one subsystem module further comprises a plurality of subsystem modules". It is not clear if the applicant is further limiting the at least one subsystem module to be more than one subsystem module (i.e. a peer

type relationship), or if the applicant is claiming that there are plural subsystem modules within the at least one subsystem module (i.e. an overlay type relationship).

Regarding claims 21 and 23, the claim recites the limitation "the plurality of optical devices". There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-4, 9-12, 15-20, 22 and 24-27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gallagher et al. (US Patent No. 5923851) in view of Yamazaki et al. (US Patent No. 5764394).

Regarding claim 1, Gallagher et al. disclose an apparatus comprising: a first bus having at least one subsystem module connected thereto (fig. 3, bus element 663 and subsystem module element 636 and col. 8, lines 7-24 and col. 9, lines 18-62), said at least one subsystem module having at least one device (element 643) which is connected to a second bus of the same protocol (i.e. ethernet) as said first bus (element 639 and col. 8, lines 7-24). Gallagher discloses the MAC layer interface connecting to the second bus (fig. 3, element 639) and connecting to an ethernet network (fig. 3, element 662), but does not disclose an optical device in the subsystem module. Yamazaki et al. disclose an optical device for interfacing an ethernet signal to an optical network, where the optical device interfaces at the MAC layer (fig. 7 and col. 5, lines 37-51). It would have been obvious to one of ordinary skill in the art at the time of the invention to make the subsystem module of Gallagher et al. an optical device by adding the

optical interface teaching of Yamazaki et al. to the Gallagher et al. subsystem module, to allow the MAC layer network interface of the Gallagher et al. subsystem module to interface with an optical network, to provide the advantage of allowing the Gallagher et al. ethernet hub to interface with an optical network (e.g. an optical LAN) since optical fiber transmission has several advantages over electrical transmission (e.g. optical fiber immunity to EMI).

Regarding claim 2, the combination of Gallagher et al. and Yamazaki et al. discloses an optical apparatus as recited in claim 1, further comprising a host processor, which is connected to a channel access table (Gallagher et al.: fig. 3, elements 629 and 627, col. 7, lines 35-49 and col. 9, lines 18-32).

Regarding claim 3, the combination of Gallagher et al. and Yamazaki et al. discloses an optical apparatus as recited in claim 2, wherein said channel access table includes a plurality of individual channel addresses (Gallagher et al.: col. 15, lines 11-22, where a "chassis port descriptor" is the individual channel address text for the channel port on the backplane – see also col. 4, lines 61-64 where a line card is a "channel"), corresponding physical addresses for each of said plurality of individual channel addresses (Gallagher et al.: col. 14, lines 27-52, where a "chassis port slot" in the "chassis port table" is a physical address of the line card "channel"), and a memory address offset for each of a plurality of individual channels (Gallagher et al.: col. 15, lines 23-47, where the offset is the "chassis connection port" as an index into the chassis port table).

Regarding claim 4, the combination of Gallagher et al. and Yamazaki et al. discloses an optical apparatus as recited in claim 1, wherein each of said at least one submodule further includes a microcontroller (Gallagher et al.: fig. 3, element 640 and col. 8, lines 7-24).

Regarding claim 9, the combination of Gallagher et al. and Yamazaki et al. discloses an optical apparatus as recited in claim 1, wherein said same protocol is chosen from the group

consisting essentially of the I.sup.2C protocol, the SPI protocol, the Ethernet protocol and the RS232 protocol (Gallagher et al.: col. 4, lines 42-55). In addition, although Ethernet is already disclosed by the combination, Applicant states in the specification "The address based shared bus interface 203 is illustratively a serial interface, for example an I.sup.2C, SPI, Ethernet, or RS232 serial interface. Of course, these interfaces are merely illustrative of the present invention and other serial interfaces may be used for the address based shared bus interface" (page 8, lines 1-4)". This is not a disclosure of criticality regarding the bus protocol. Absent a teaching of criticality for the bus protocol, the claimed protocols would have been the result of obvious engineering design choice.

Regarding claim 10, the combination of Gallagher et al. and Yamazaki et al. discloses an optical apparatus as recited in claim 2, wherein said host processor calculates a command and data bytes (col. 20, lines 56-63, where the SET command and its data -- i.e. "values or codes" -- for a line card are the command and data bytes). The combination does not explicitly describe a "virtual access syntax" which includes a channel address and memory address. However, it would have been obvious to one of ordinary skill in the art at the time of the invention that the disclosed chassis table information described for claim 3, including the "chassis port descriptors" and "chassis connection ports", would be used by the management agent microprocessor in an access syntax when gathering information from the line cards and sending commands to the individual line cards.

Regarding claim 11, the combination of Gallagher et al. and Yamazaki et al. discloses an optical apparatus as recited in claim 3, but does not explicitly describe a "physical access syntax". However, it would have been obvious to one of ordinary skill in the art at the time of the invention that the disclosed chassis table information described for claim 3, including the

"chassis port slot" corresponding to the physical slot ID, would be used by the management agent microprocessor in an access syntax for accessing the individual line cards.

Regarding claim 12, the combination of Gallagher et al. and Yamazaki et al. discloses an optical apparatus as recited in claim 11, wherein said host processor calculates a command and data bytes (col. 20, lines 56-63, where the SET command and its data -- i.e. "values or codes" -- for a line card are the command and data bytes). The combination does not explicitly describe a "physical access syntax" which includes a physical address and memory address. However, it would have been obvious to one of ordinary skill in the art at the time of the invention that the disclosed chassis table information described for claim 3, including the "chassis port slots" and "chassis connection ports", would be used by the management agent microprocessor in an access syntax gathering information from the line cards and sending commands to the individual line cards.

Regarding claim 15, the combination of Gallagher et al. and Yamazaki et al. discloses an optical apparatus as recited in claim 1, wherein said at least one optical device is chosen from the group consisting essentially of transmitters, receivers, transceivers and transponders (Gallagher et al.: col. 5, lines 37-51).

Regarding claim 16, Gallagher et al. disclose a method of accessing a plurality of devices, the method comprising: translating a channel address to a physical access address with a memory offset (Gallagher et al.: col. 15, lines 11-22, where a "chassis port descriptor" is the individual channel address text for the channel port on the backplane; and col. 14, lines 27-52, where a "chassis port slot" in the "chassis port table" is a physical address of the line card; and col. 15, lines 23-47, where the offset is the "chassis connection port" as an index into the chassis port table). Gallagher discloses the MAC layer interface connecting to the second bus (fig. 3, element 639) and connecting to an ethernet network (fig. 3, element 662), but does not

disclose an optical device in the subsystem module. Yamazaki et al. disclose an optical device for interfacing an ethernet signal to an optical network, where the optical device interfaces at the MAC layer (fig. 7 and col. 5, lines 37-51). It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teaching of Yamazaki et al. with Gallagher as described above for claim 1.r

Regarding claim 17, the combination of Gallagher et al. and Yamazaki et al. discloses a method as recited in claim 16, wherein said translating further comprises using a channel access table (Gallagher et al.: fig. 3, elements 629 and 627, col. 7, lines 35-49 and col. 9, lines 18-32).

Regarding claim 18, the combination of Gallagher et al. and Yamazaki et al. discloses a method as recited in claim 16, but does not explicitly describe a "virtual access syntax". However, it would have been obvious to one of ordinary skill in the art at the time of the invention that the disclosed chassis table information described for claim 3, including the "chassis port descriptors" and "chassis connection ports", would be used by the management agent microprocessor in an access syntax when gathering information from the line cards and sending commands to the individual line cards.

Regarding claim 19, the combination of Gallagher et al. and Yamazaki et al. discloses a method as recited in claim 18, but does not explicitly describe a "physical access syntax". However, it would have been obvious to one of ordinary skill in the art at the time of the invention that the disclosed chassis table information described for claim 3, including the "chassis port slot" corresponding to the physical slot ID, would be used by the management agent microprocessor in an access syntax for accessing the individual line cards.

Regarding claim 20, the combination of Gallagher et al. and Yamazaki et al. discloses a method as recited in claim 19, wherein said host processor accesses a channel access table

(Gallagher et al.: fig. 3, elements 629 and 627 and col. 7, lines 35-49) to calculate said physical access syntax (Gallagher et al.: col. 14, lines 27-52, where a "chassis port slot" in the "chassis port table" is a physical address of the line card).

Regarding claim 22, the combination of Gallagher et al. and Yamazaki et al. discloses a method as recited in claim 17, wherein said channel access table includes a plurality of individual channel addresses (Gallagher et al.: col. 15, lines 11-22, where a "chassis port descriptor" is the individual channel address text for the channel port on the backplane – see also col. 4, lines 61-64 where a line card is a "channel"), corresponding physical addresses for each of said plurality of individual channel addresses (Gallagher et al.: col. 14, lines 27-52, where a "chassis port slot" in the "chassis port table" is a physical address of the line card "channel"), and a memory address offset for each of a plurality of individual channels (Gallagher et al.: col. 15, lines 23-47, where the offset is the "chassis connection port" as an index into the chassis port table).

Regarding claim 24, the combination of Gallagher et al. and Yamazaki et al. discloses a method as recited in claim 16, wherein a host processor performs said translating (Gallagher et al.: fig. 3, elements 629 and 627 and col. 7, lines 35-49, wherein the translating includes using the channel access tables which are accessed by the host processor).

Regarding claim 25, the combination of Gallagher et al. and Yamazaki et al. discloses a method as recited in claim 16, wherein the accessing further comprises reading data from said plurality of optical devices (Gallagher et al.: col. 20, lines 45-55).

Regarding claim 26, the combination of Gallagher et al. and Yamazaki et al. discloses a method as recited in claim 16, wherein the accessing further comprises writing data to said plurality of optical devices (Gallagher et al.: col. 20, lines 56-63).

Regarding claim 27, the combination of Gallagher et al. and Yamazaki et al. discloses a method as recited in claim 16, where the external network interfacing is done optically. The Applicant states in the specification "In the illustrative embodiment shown in Fig. 2(b), the transmitters are the individual transmitters of a DWDM system. Of course, this is merely illustrative, and as can be readily appreciated, other devices for use in other types of communication schemes may be used. For example, the individual devices may be transceivers, transponders or individual receivers, instead of or in addition to the illustrative transmitters" (page 9, lines 15-20). This is not a disclosure of criticality regarding the optical devices being part of a WDM system. Absent a teaching of criticality for the optical devices being WDM components, using the optical devices for WDM would have been the result of obvious engineering design choice.

Conclusion

6. Any inquiry concerning this communication from the examiner should be directed to N. Curs whose telephone number is (571) 272-3028. The examiner can normally be reached M-F (from 9 AM to 5 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jason Chan, can be reached at (571) 272-3022. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (571) 272-2600.

M. R. Sedighian

M. R. SEDIGHIAN
PRIMARY EXAMINER